2N4351 (SILICON)

MOTOROLA

CASE 20(2)
(TO-72)

Silicon N-channel MOS field effect transistors, designed for enhancement-mode operation in low power switching applications. The 2N4351 is complementary with type 2N4352 .

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Gate-Source Voltage	V_{GS}	± 30	Vdc
Drain Current	I_D	30	mAdc
Power Dissipation at T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
Power Dissipation at T_C = 25°C Derate about 25°C	P_D	800 4.56	mW mW/°C
Operating Junction Temperature	T_J	175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

HANDLING PRECAUTIONS:

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

2N4351 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Substrate connected to source.

Characteristic	Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μA, V_{GS} = 0)	—	$V_{(BR)DSS}$	25	—	Vdc
Gate Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)	—	I_{GSS}	—	10	pAdc
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0)	—	I_{DSS}	—	10	nAdc
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V_{DS} = 10 V, I_D = 10 μA)	—	$V_{GS(TH)}$	1.0	5	Vdc
"ON" Drain Current (V_{GS} = 10 V, V_{DS} = 10 V)	3	$I_{D(on)}$	3	—	mAdc
Drain-Source "ON" Voltage (I_D = 2 mA, V_{GS} = 10 V)	—	$V_{DS(on)}$	—	1.0	Vdc
SMALL SIGNAL CHARACTERISTICS					
Drain-Source Resistance (V_{GS} = 10 V, I_D = 0, f = 1 kHz)	4	$r_{ds(on)}$	—	300	ohms
Forward Transfer Admittance (V_{DS} = 10 V, I_D = 2 mA, f = 1 kHz)	1	$\lvert y_{fs} \rvert$	1000	—	μmho
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	2	C_{rss}	—	1.3	pF
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz)	2	C_{iss}	—	5.0	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz)	—	$C_{d(sub)}$	—	5.0	pF
SWITCHING CHARACTERISTICS					
Turn-On Delay	I_D = 2.0 mAdc, V_{DS} = 10 Vdc, V_{GS} = 10 Vdc (See Figure 10; Times Circuit Determined)	6, 10	t_{d1}	—	45	ns
Rise Time		7, 10	t_r	—	65	ns
Turn-Off Delay		8, 10	t_{d2}	—	60	ns
Fall Time		9, 10	t_f	—	100	ns

FIGURE 1 — FORWARD TRANSFER ADMITTANCE

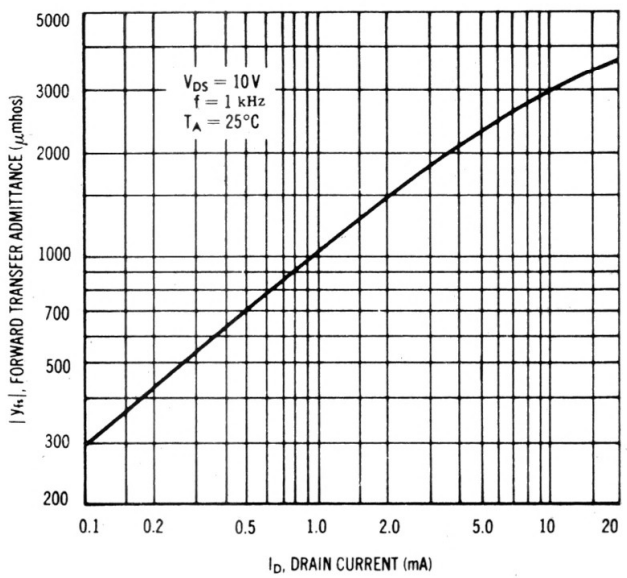


FIGURE 2 — CAPACITANCE

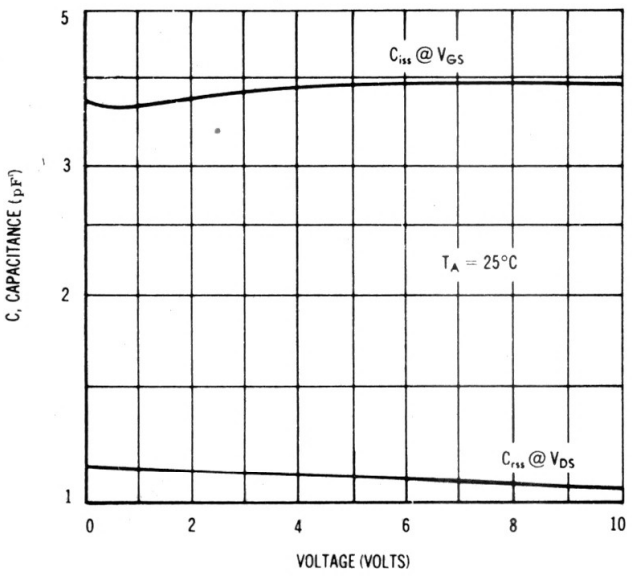


FIGURE 3 — TRANSFER CHARACTERISTICS

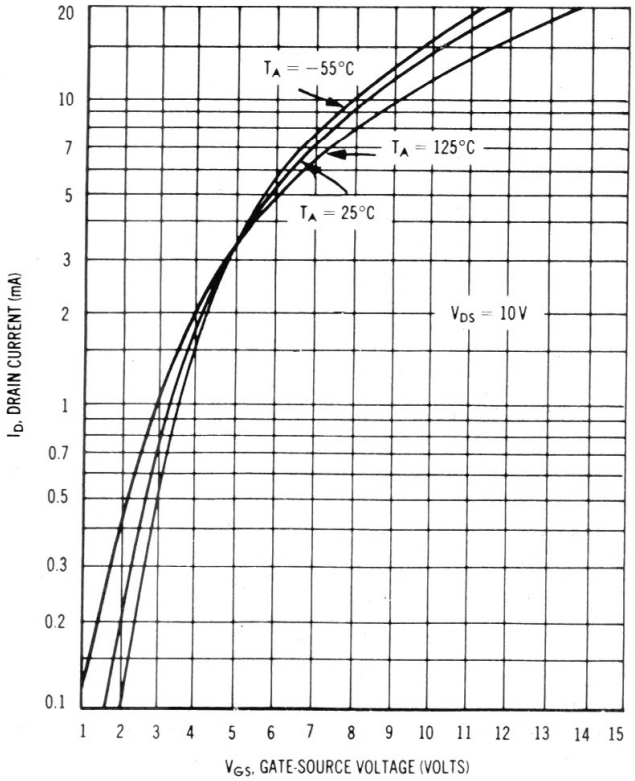


FIGURE 4 — DRAIN SOURCE "ON" RESISTANCE

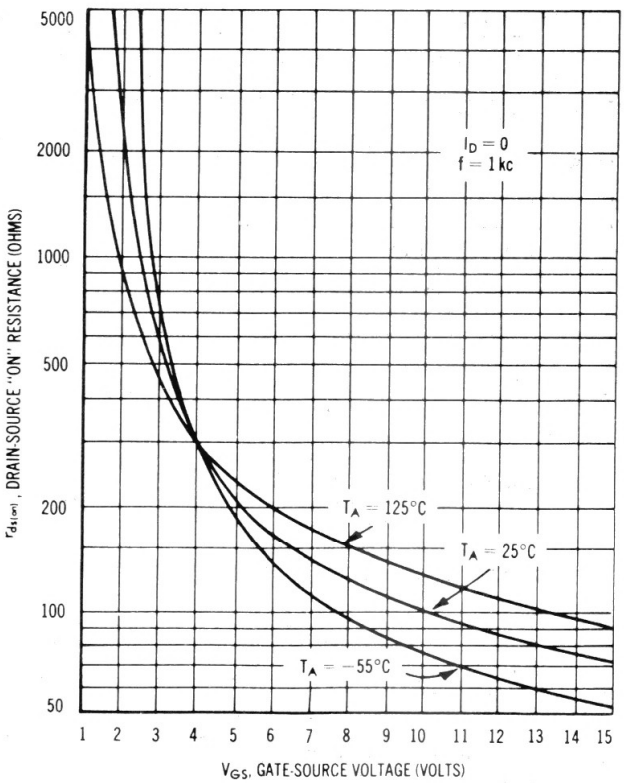
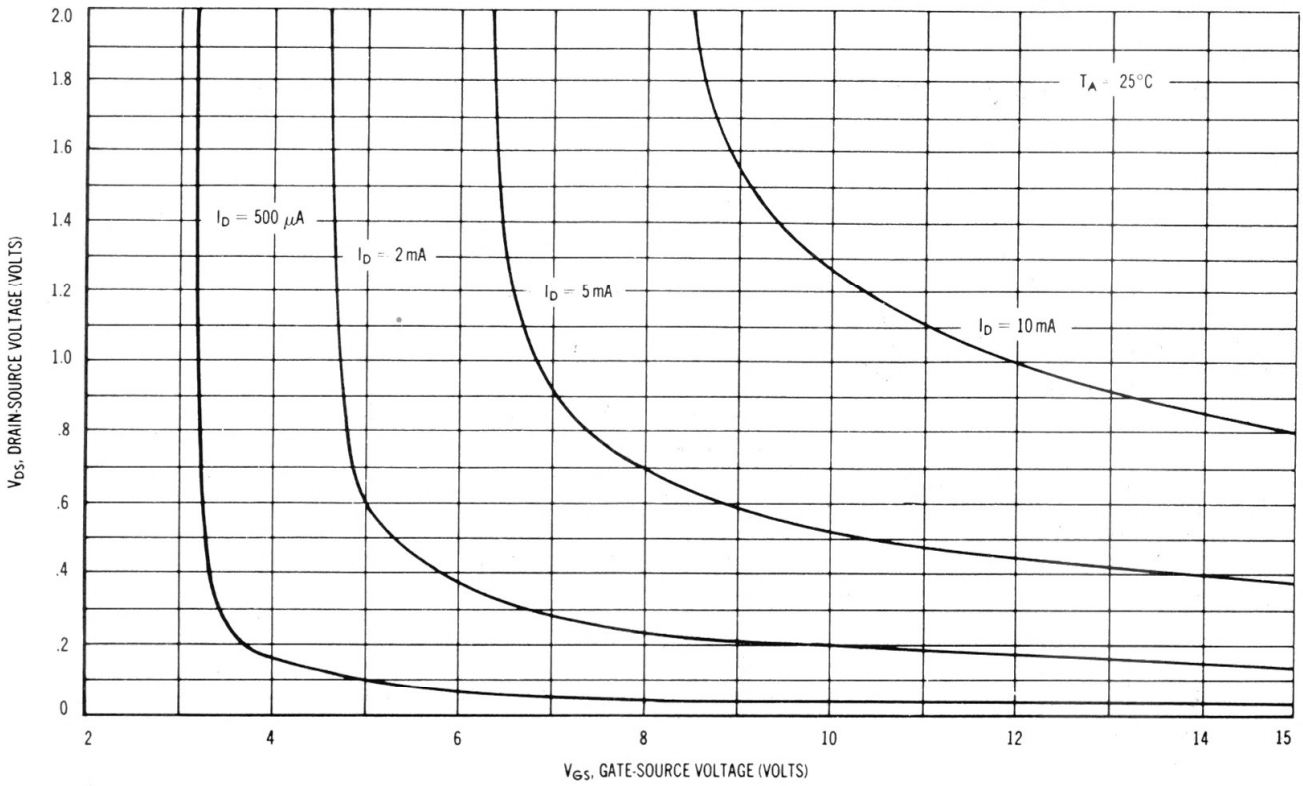


FIGURE 5 — "ON" DRAIN-SOURCE VOLTAGE



2N4351 (continued)

SWITCHING CHARACTERISTICS

($T_A = 25°C$)

FIGURE 6 — TURN-ON DELAY TIME

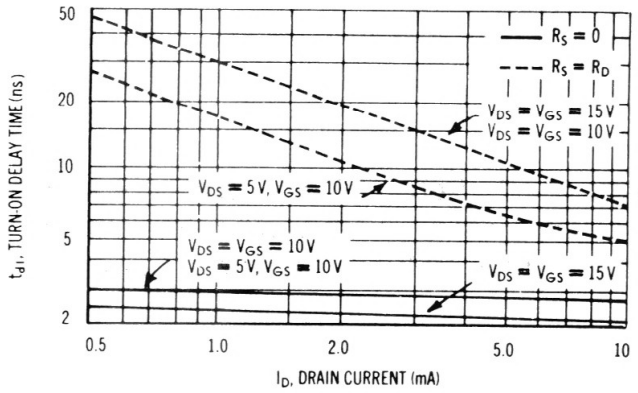


FIGURE 7 — RISE TIME

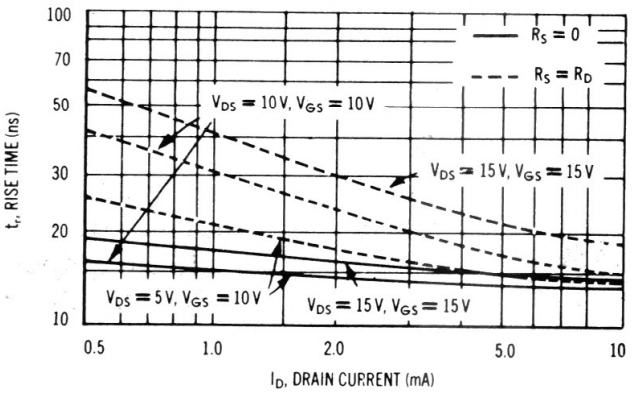


FIGURE 8 — TURN-OFF DELAY TIME

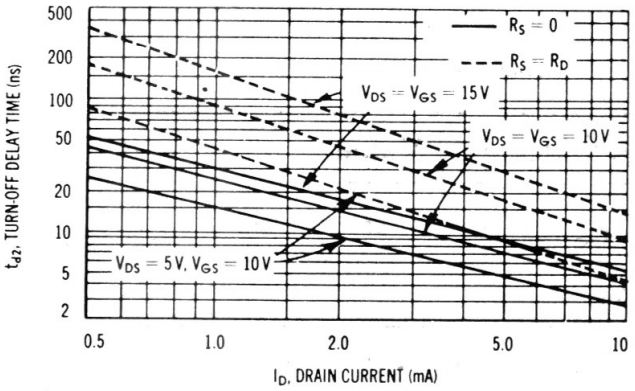


FIGURE 9 — FALL TIME

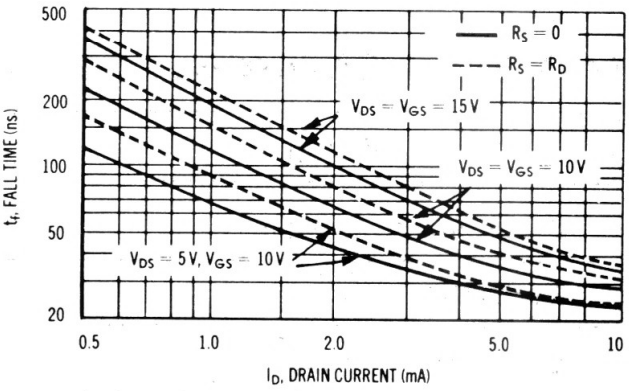


FIGURE 10 — SWITCHING CIRCUIT and WAVEFORMS

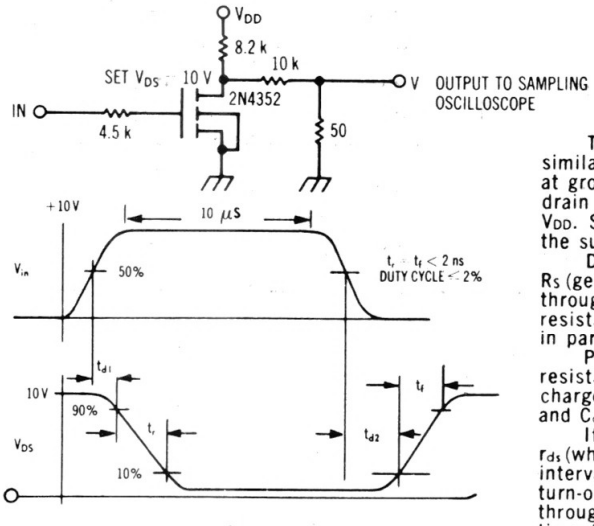
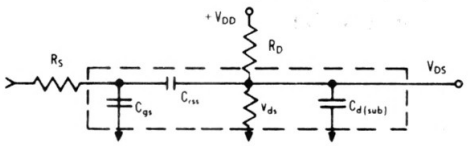


FIGURE 11 — SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL



The switching characteristics shown above were measured in a test circuit similar to Figure 10. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{iss} - C_{rss}$) has no charge. The drain voltage is at V_{DD}, and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_S (generator impedance) (Figure 11). C_{rss} must be discharged to $V_{GS} - V_{D(on)}$ through R_S and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 4) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_S = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_S = R_D$ simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_S = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.